



ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

DESIGN OF A SYNCHRONOUS SUPERREGENERATIVE RECEIVER AT 2.4 GHz

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1. PROJECT DESCRIPTION

1.1. Introduction

Superregenerative receivers have been used for many decades in short-distance wireless communications due to their simplicity, reduced cost and low power consumption. Typical applications include: remote control systems (such as garage door openers, car alarms, robotics, model ships and airplanes, etc.), short-distance telemetry, medical instrumentation, cordless telephones and the like. In the present project, the design of a superregenerative receiver operating in the 2.4-GHz ISM band is proposed. Additionally, the performances of a new quench technique will be investigated.

1.2. Operation of a conventional superregenerative receiver

Conventional superregenerative receivers operating under OOK modulated signals usually take many samples of each received bit in an asynchronous manner. The bit value is detected by later integration of these samples (Fig. 1). The advantages of this mode of operation are that tuning and high gain can be achieved with a simple and low-power-consumption receiver. However, the RF bandwidth of the receiver results much greater than the modulation bandwidth, making the receiver less immune to noise and interference than other receiver types, such as superheterodyne receivers.

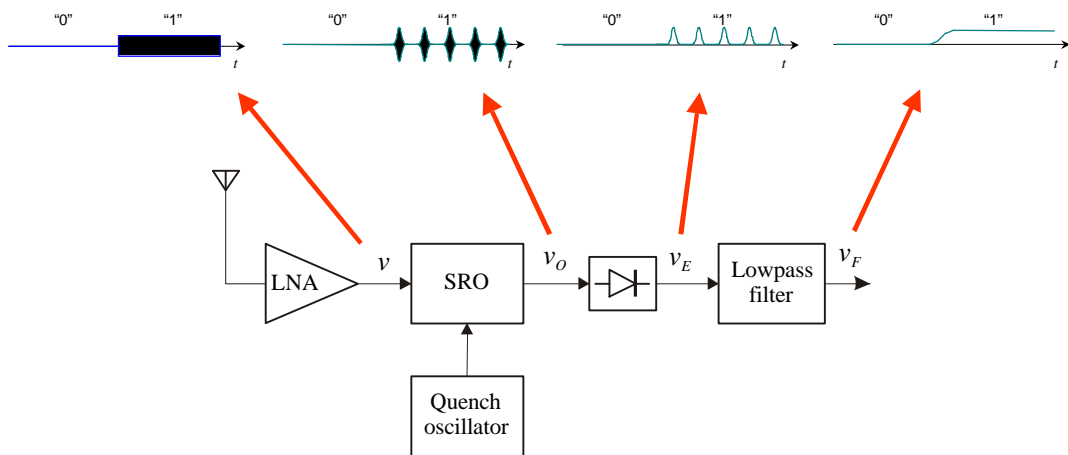


Figure 1. Block diagram and typical signals in a conventional superregenerative receiver.

1.3. The synchronous quench: a new mode of operation

A number of enhancements can be obtained by quenching the superregenerative oscillator (SRO) a single time per bit period, so that only one sample of each received bit is taken. This mode of operation requires the generation of a control signal that drives the quench oscillator in order to maintain synchronism with the received signal. Fig. 2 illustrates the two modes of operation.

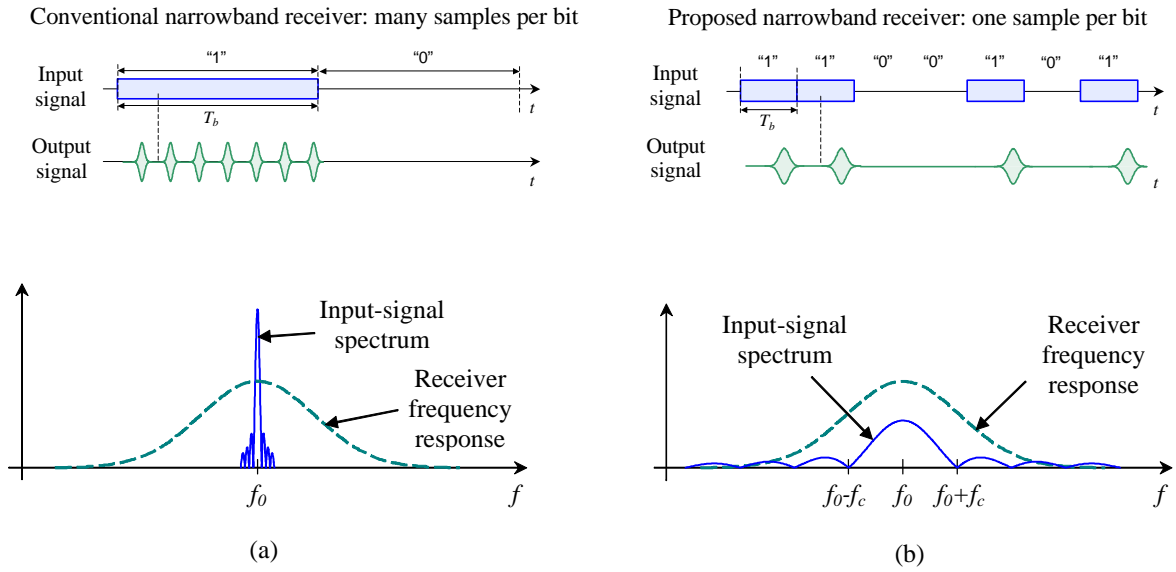


Figure 2. (a) Asynchronous and (b) synchronous operation of the superregenerative oscillator.

According to conclusions obtained for spread-spectrum superregenerative receivers in [Mon-02], by using special bit envelopes it is possible to achieve many improvements on the conventional receiver, namely:

- 1) The receiver bandwidth can match that of the input signal.
- 2) Better sensitivity, since the received energy can be concentrated in the characteristic sensitive periods of the receiver. An improvement of 8 to 10 dB is typically obtained.
- 3) Improved rejection to narrowband interference.
- 4) Reduced data jitter, due to the synchronous operation of the receiver.

- 5) Increased data rate, since it is equal to the quench frequency f_q and no longer a fraction of it.

Example: Operation in the 2.4 GHz ISM band using a low- Q resonator

$$\left. \begin{array}{l} f_0 = 2.4 \text{ GHz} \\ Q_0 = 10 \end{array} \right\} \rightarrow f_{qmax} \approx \frac{f_0}{100} = 24 \text{ MHz} \rightarrow 24 \text{ Mbps !!!}$$

1.4. Synchronization techniques

A loop that controls the frequency of the quench oscillator is necessary in order to maintain synchronism. Precisely, in [Mon-02] several synchronization techniques have been successfully implemented, some of them especially simple. In all cases, the control signal is obtained using the sensitive periods of the superregenerative oscillator in combination with specific shapes of the bit envelope (Fig. 3). The block diagrams of the corresponding architectures for a narrowband receiver are presented below. Additional information can be found in the above-mentioned reference.

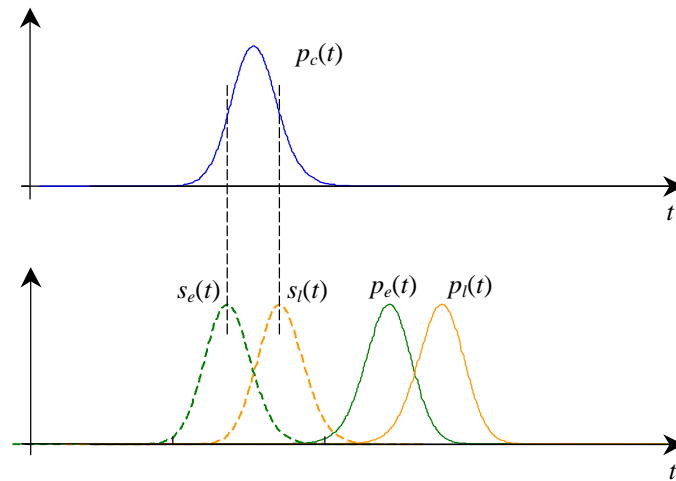


Figure 3. Advanced (*early*) and delayed (*late*) sensitive periods for the generation of a phase-discrimination characteristic ($p_c(t)$: received bit envelope; $s(t)$: sensitivity curve; $p(t)$ envelope of the superregenerative oscillator output).

Delay-Locked Loop (DLL)

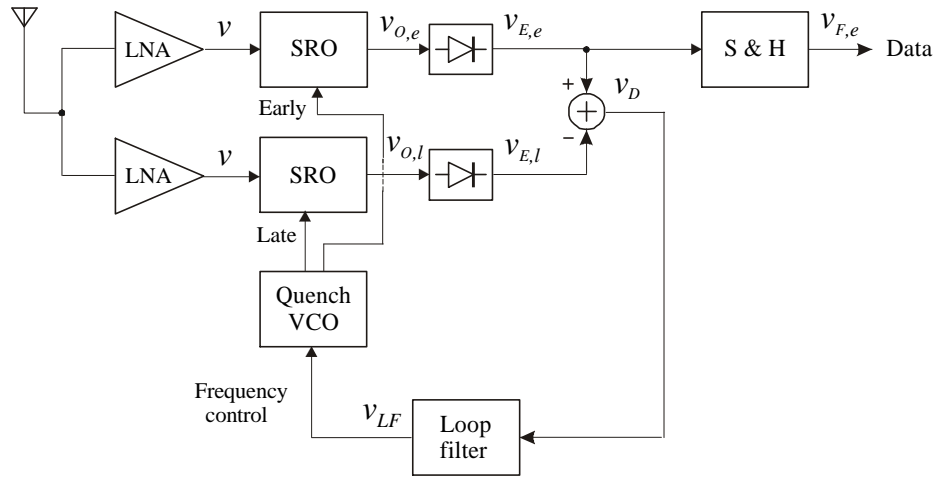


Figure 4

Advantages:

- Efficient use of the incoming signal power.

Tau-Dither Loop (TDL)

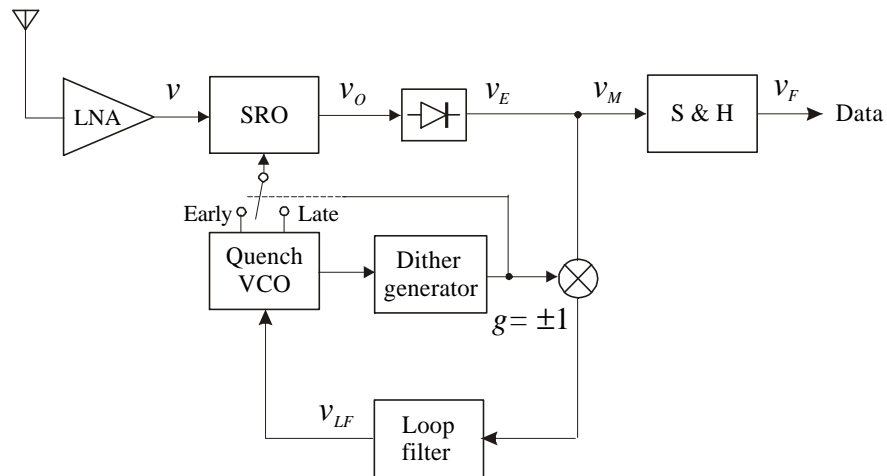


Figure 5

Advantages:

- Simplicity;
- No double RF path, no crosstalk between early and late channels.

Single-Flank Delay-Locked Loop (SF DLL)

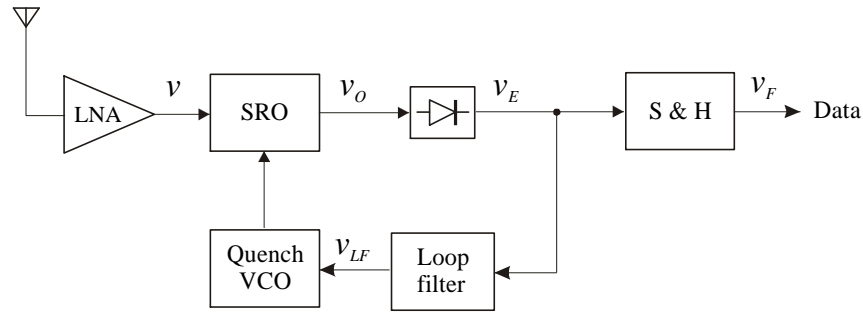


Figure 6

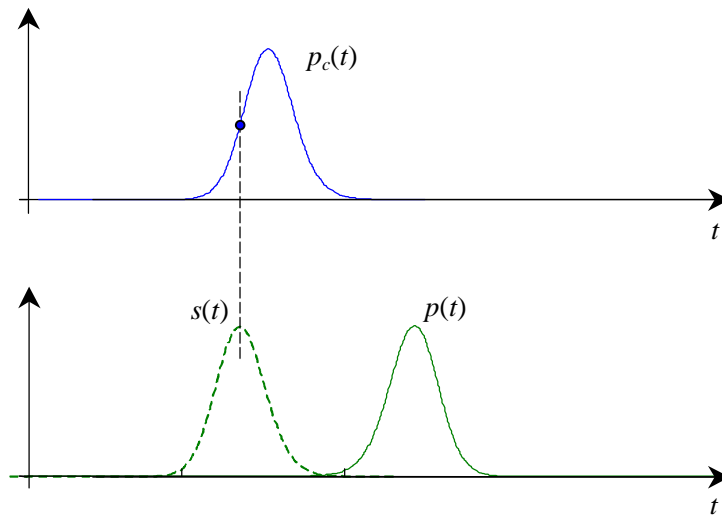


Figure 7. Sensitivity curve of a Single-Flank superregenerative DLL aligned to its equilibrium point.

Advantages:

- Extremely simple;
- Experimental results for spread-spectrum receivers show very good acquisition and tracking performances, with good sensitivity and large input dynamic range;
- Output level independent on the input amplitude. However, the tracking error depends significantly on the input amplitude (the use of AGC and/or special purpose loop filters might mitigate this).

1.5. Project objectives

- 1) Implementation of a selected architecture and evaluation of its performance.
The unlicensed ISM band of 2.4 GHz is targeted due to its worldwide availability.
- 2) Optimization, paying special attention to:
 - . The superregenerative oscillator
 - . The synchronization loop;
- 3) Publication of results: elaboration of a paper to be submitted to a journal and/or to a symposium.

1.6. Planning

1st Month:

- Get in touch, planning and beginning of the design.

2nd Month:

- Development and completion of the design.
- Evaluation of performance and optimization.

3rd Month:

- Final measurements and conclusions.
- Preparation of a paper to be submitted to a conference and/or to a journal, which will be signed by the people involved in the project.

2. DESIGN AND IMPLEMENTATION OF THE RF MODULE

2.1. Preliminary considerations

The RF module includes the low-noise amplifier (LNA), the superregenerative oscillator (SRO) and the envelope detector (see figures 1, 4, 5, and 6). This module is expected to satisfy many requirements:

- 1) It must be able to operate in the 2.4-GHz ISM band (2400 to 2483.5 MHz);
- 2) It must work with RF input signal levels as low as possible, i.e., its sensitivity must be optimized;
- 3) Its power consumption must be minimized;
- 4) The level of the demodulated output signal, provided by the envelope detector, must be large enough so that it can be easily amplified and processed.

The RF module has been designed to operate with a supply voltage of 3 V, which is the selected voltage for the whole receiver. However, according to the characteristics of the employed active device, operation at supply voltages of 1 V or less seems feasible. This requires redesigning the biasing network of each stage. The most critical part will be the cascode used in the LNA, because of the two-transistor configuration.

2.2. Selection of the active device

The characteristics of the active devices play a fundamental role in the overall performance of the receiver. After comparing several high-frequency transistors, including the 25-GHz-transition-frequency BFP420 and BFP405 transistors from Infineon Technologies, the BFP405 has been chosen. This transistor is very well suited for low current applications, since it exhibits a high transition frequency as well as an outstanding power gain at very low biasing currents. In addition, its parasitic capacitances are low and its noise figure, of about 1.5 dB at 2.4 GHz, is also good. Table 1 compares the features of BFP420 and BFP405 with a biasing current of 0.5 mA.

Table 1 – Features of BFP420 and BFP405 transistors at 2.4 GHz and $I_c=0.5$ mA.

<i>Parameter</i>	BFP420	BFP405	<i>Units</i>
Noise figure	1.7	1.6	dB
Power gain	12	13	dB
Transition frequency	~3	5	GHz
Collector-base capacitance	0.15	0.05	pF
Emitter-base capacitance	0.55	0.29	pF
Collector-emitter capacitance	0.37	0.24	pF

2.3. Steps made in the completion of the design

The tool used for simulation is Advanced Design System (ADS) from Agilent Technologies. It has been a key in obtaining a successful result. The following steps have been made to complete the final design.

- 1) ADS schematic simulation: exhaustive simulation of several configurations for the LNA, the SRO and the envelope detector has been carried out, including common-base, common-emitter and common-collector configurations. The ADS manufacturer's models of the transistors, the capacitors and the inductors have been used to obtain a more realistic simulation.
- 2) PCB design: The PCB design of the selected configurations has been done with Protel 99 SE. The size of the layout has been minimized in order to reduce the influence of parasitic capacitances and inductances associated to the terminal connections. Grounded DC-blocks have been placed at each supply node, whereas chokes have been included to isolate RF nodes from external supply and quench terminals.
- 3) ADS layout simulation: A layout has been generated in ADS according to the designed PCB. Large ground planes on the top layer have been removed in order to reduce computation load. The layout has been simulated electromagnetically with *Momentum* (microwave mode) as follows:
 - a) Ports have been added to the layout to allow the connection of discrete devices;

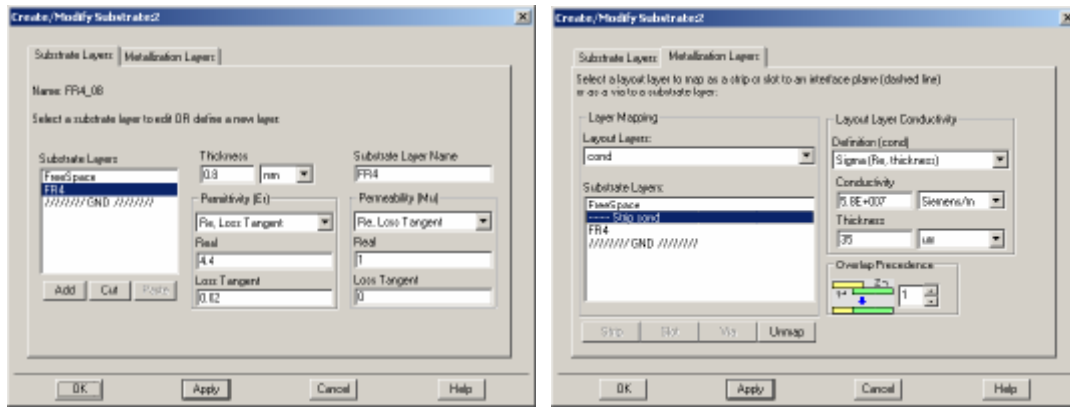
- b) The characteristics of the substrate and metallization layers have been introduced:
 - Substrate layer: FR4 type, thickness=0.8 mm, $\epsilon_r=4.4$, $\tan\delta=0.02$;
 - Metallization layer: Copper, thickness=0.35 μm , $\sigma=5.8\times 10^7 \Omega^{-1}/\text{m}$;
- c) Mesh parameters have been specified:
 - Mesh frequency: 3.5 GHz;
 - Mesh density: 30 cells/wavelength;
 - Arc resolution: 45 degrees.
- d) S-parameters have been calculated following the frequency plans:
 - Single point at 0 Hz (DC simulation);
 - 11 points from 1.5 to 3.5 GHz;
 - 11 points from 2.3 to 2.6 GHz;
- e) The simulated layout has been added to the ADS component library;
- f) The new component has been simulated in a schematic window after connecting the discrete devices to the corresponding ports.

Fig. 8 shows some of ADS windows with the selected parameters. In Fig. 9, the schematic of the PCB layout with the discrete components connected is presented.

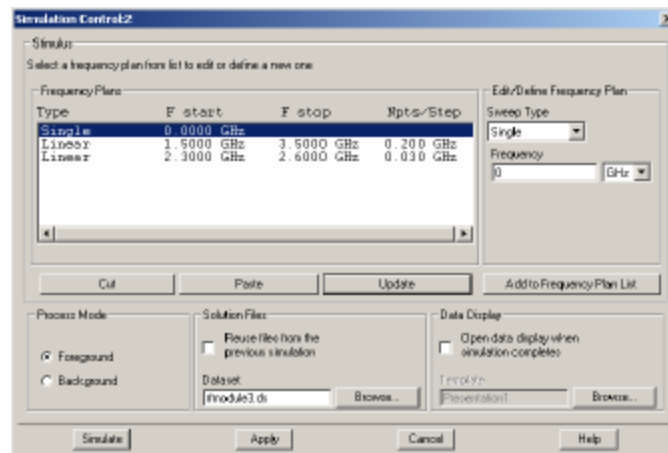
Simulation with Momentum is with no doubt the most critical part of the process. It may take many hours. Linear frequency plans have been used due to computer-hanging problems when using adaptive plans.

The main differences that have been observed in layout simulation with regard to schematic simulation (without layout) are the following:

- Increased circuit losses due to substrate losses. Therefore, noise figure and resonator Q degrade, whereas the current consumption of the oscillator tends to increment;
- Increased input and output capacitance in each RF stage. This is caused by the finite surface associated to the small microstrip connections between components. As a result, the resonant frequency of the system is reduced.



(a)



(b)

Figure 8. (a) Windows for setting the characteristics of substrate and metallization layers; (b) frequency plans used in simulation with Momentum.

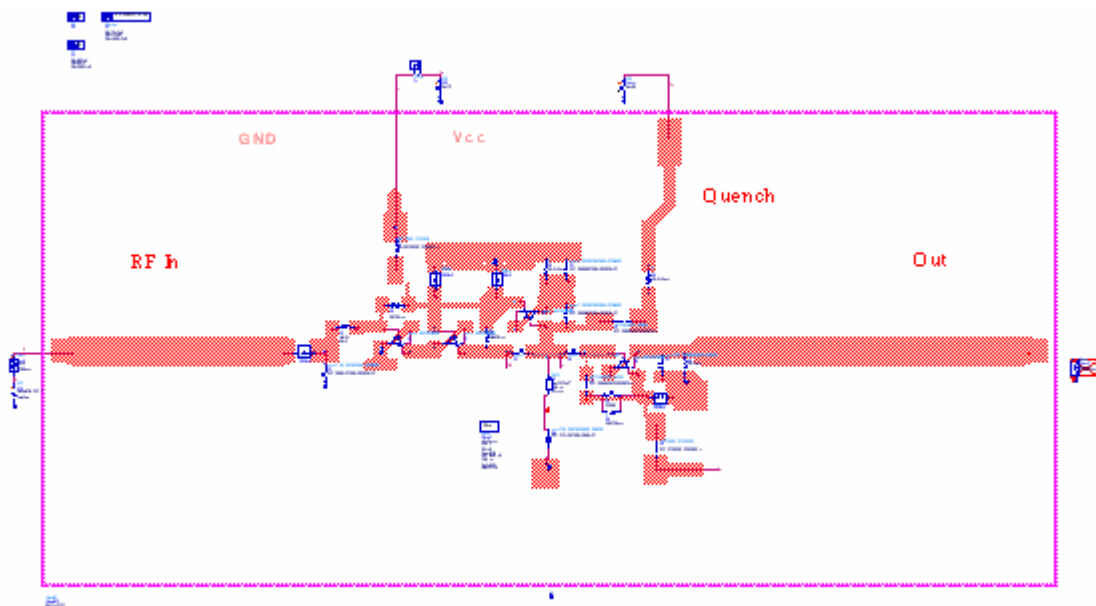


Figure 9. ADS layout component with the discrete components connected.

- 4) Implementation and experimental verification: Exhaustive measurements have been made in the laboratory to verify simulation predictions. Several operating conditions for the different stages have been evaluated in order to obtain the best performance. Hence, minimum supply current providing the best noise figure for the LNA has been applied. Several input matching networks for minimum noise figure have been evaluated. Regarding the envelope detector, several biasing currents have been applied and different values of RC time constant have been tested to obtain relatively high output amplitude.

2.4. Low-noise amplifier

The primary goals in the design of the LNA have been:

- To minimize its noise figure;
- To achieve high reverse isolation;
- To provide good matching between the antenna impedance ($50\ \Omega$) and the SRO impedance ($\sim 1\ \text{k}\Omega$ at resonance);
- To achieve relatively high signal gain in order to minimize the effect of noise generated by the SRO.

The theory of superregenerative receivers shows that the voltage generated across the SRO under normal quench operation is proportional to that generated when the

Table 2 – Comparison of several LNA configurations using BFP405 (ADS schematic simulation).

<i>Configuration</i>	<i>Noise figure (dB)</i>	<i>Gain (dB)</i>	<i>Reverse isolation (dB)</i>
Common emitter			
$I_c=200\ \mu\text{A}$	1.1	20	16
$I_c=400\ \mu\text{A}$	1.1	22	18
Common base			
$I_c=200\ \mu\text{A}$	1.5	8	26
$I_c=400\ \mu\text{A}$	1.5	10	28
Cascode			
$I_c=200\ \mu\text{A}$	3	21	32
$I_c=400\ \mu\text{A}$	1.7	28	38

quench signal is disabled, i.e., when there is no compensation of tank losses [Mac-46]. Hence, the gain and the noise figure of the LNA loaded with the SRO can be calculated using the model of the passive resonator connected to the LNA output.

A common-emitter amplifier has been simulated, offering a reverse isolation of about 20 dB with a bias current of 500 μA . With a common-base amplifier, which offers typically higher isolation, we get near 30 dB. A cascode configuration, shown in Fig. 10, has been chosen thanks to its good reverse isolation of about 40 dB. Although this configuration uses two transistors, the current consumption is the same as with single-transistor configurations. However, the noise figure increases slightly. This figure degrades quite more rapidly as the supply current is decreased, in comparison with single-transistor configurations, as shown in Table 2.

Optimization of the noise figure

The cascode (Fig. 10) has been optimized to achieve a minimum noise figure of 2.5 dB. This requires a relatively high consumption of 460 μA (Table 3). The consumption can be decreased at the price of both signal gain and reverse isolation reductions and also of an increase in the noise figure. According to ADS, the noise figure of 1.7 dB in the schematic simulation increases to 2.5 dB in the layout simulation. This increase can be attributed to substrate losses present in the input microstrip line and matching network.

Fig. 11 shows the source impedance that minimizes the noise figure (layout simulation). It must be mentioned that the value of this impedance is quite different from that calculated with the schematic. Fig. 12 shows the noise figure without and with the input matching network. The matching network (CL1 and LL1) produces an improvement of 3 dB. The presence of the matching network causes:

- A reduction of noise figure;
- An increase of signal gain;
- A reduction of reverse isolation.

Fig. 13 plots the forward and reverse voltage gains as a function of frequency. The gain of the LNA loaded with the SRO and the envelope detector is quite larger than the one obtained on a pure resistive load. This is due to the inductive impedance of the load at the resonance frequency, which cancels the parasitic output capacitance of the LNA.

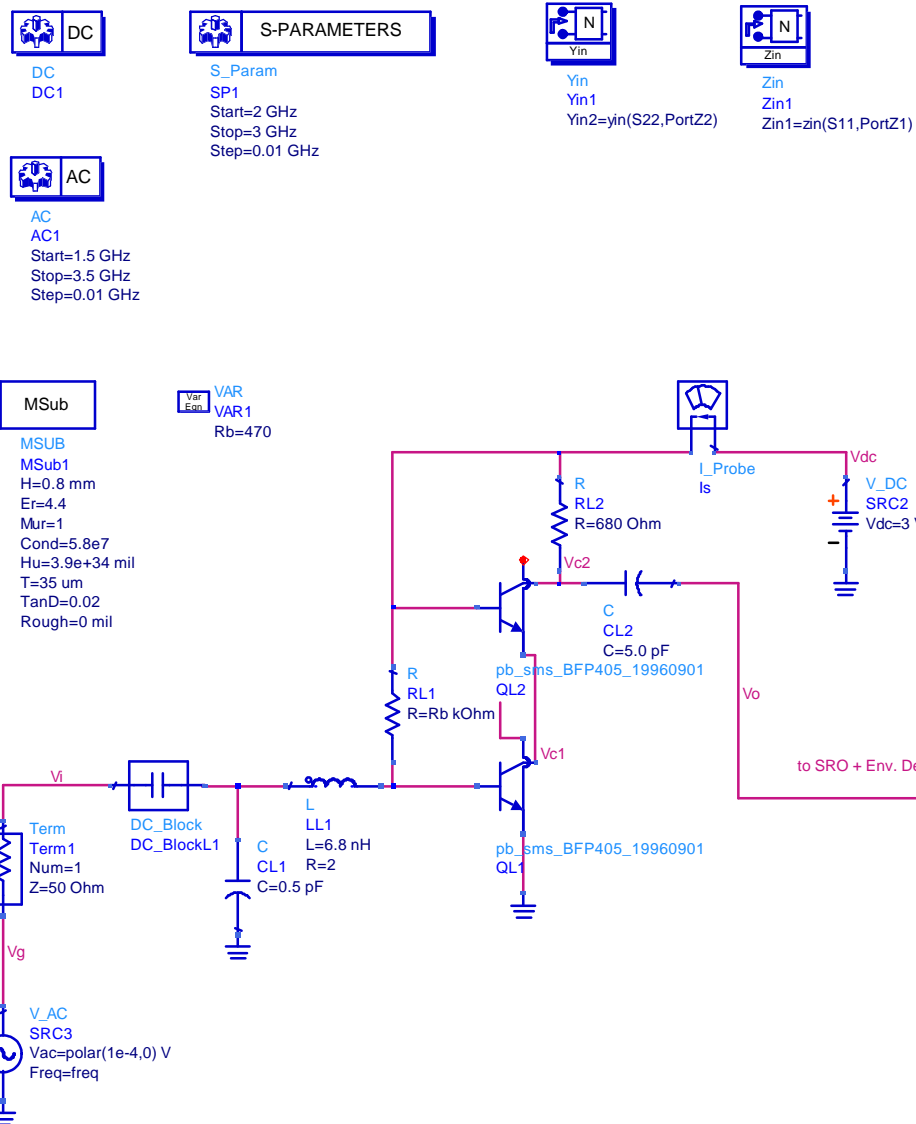


Figure 10. Schematic of the implemented cascode *.

Table 3 – Cascode features for different supply currents (ADS layout simulation).

<i>LNA supply current</i> (μA)	<i>Noise figure</i> (dB)	<i>Gain</i> (dB)	<i>Reverse isolation</i> (dB)
200	5	17	35
460	2.5	27	40

* Note: ideal capacitors and inductors are presented in this and other schematics for the sake of graphic readability; manufacturer's models have been used in simulation.

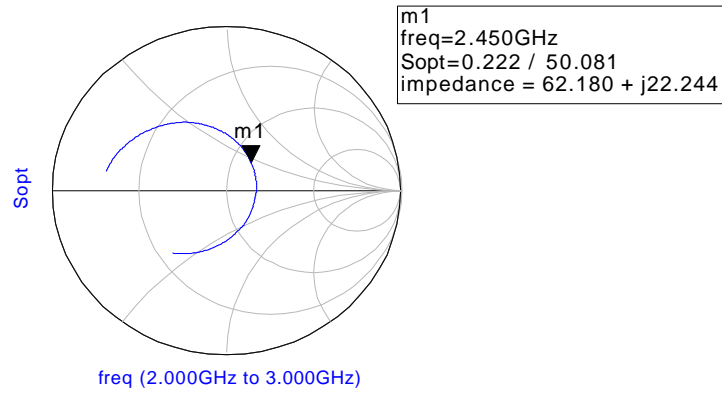


Figure 11. Optimum source impedance for minimum noise figure (ADS layout simulation).

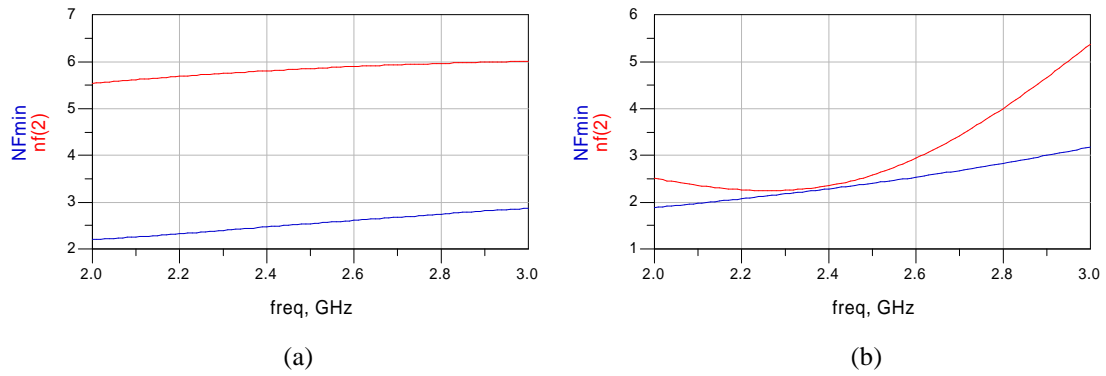


Figure 12. Actual noise figure and minimum noise figure of the simulated layout: (a) without input matching network; (b) with input matching network.

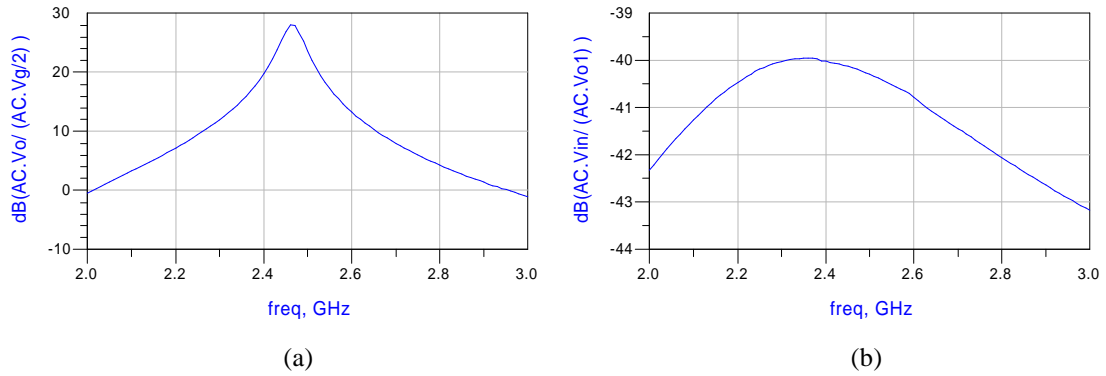


Figure 13. (a) LNA forward voltage gain (relative to reference input voltage on a 50-Ω impedance) and (b) reverse voltage gain.

Output impedance

Fig. 14 shows the output parallel resistance and capacitance of the cascode. The 680-Ohm collector resistor replaces an RF choke in order to obtain an output parallel resistance greater than 7.5 k Ω within the working band. Otherwise, with an RF choke the output resistance becomes negative and there exists risk of instability (eventually, this property could be exploited to increase the Q of the loaded SRO). A value larger than 7.5 k Ω ensures a small loading effect on the SRO. Remarkable differences are obtained in the output impedance between schematic simulation (0.2 pF // 2.2 k Ω) and layout simulation (0.47 pF // 15 k Ω) at the 2.45-GHz frequency. The common-base transistor operates near saturation with a collector DC voltage lower than the base voltage. Care must be taken to avoid saturation whether the DC current collector or the collector resistance is increased. A solution to this problem is to place a choke in parallel with the collector resistance.

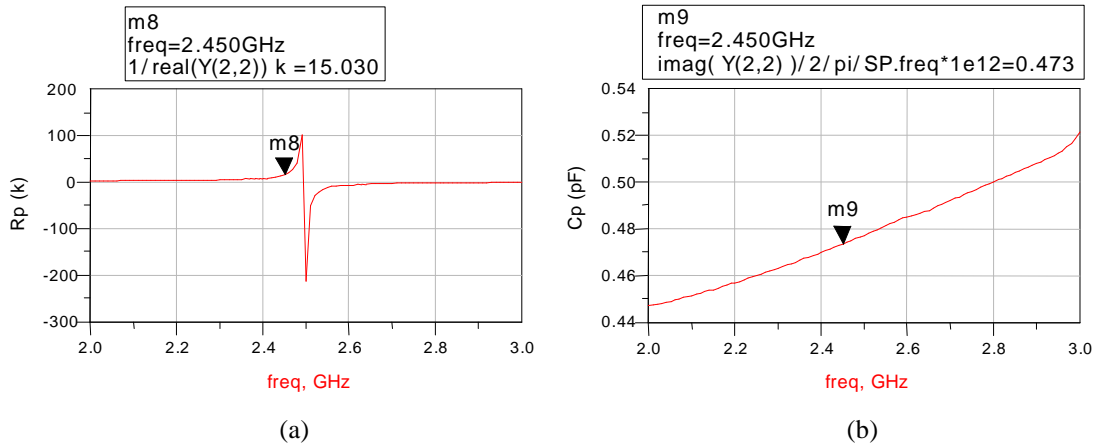


Figure 14. (a) LNA parallel output resistance; (b) parallel output capacitance.

2.5. Superregenerative oscillator

Several configurations of SRO have been evaluated. An oscillator based on a transistor amplifier fed back with coupled microstrip lines seems a good choice in order to reduce the influence of parasitic effects. Simulation shows that this configuration works with relatively long microstrip lines (2-3 cm). However, the impedance matching between the feedback network and the amplifier becomes a problem rather complex,

and the control of the loaded Q is difficult. As well, a delay line must be included to satisfy the Nyquist/Barkhausen criterion.

The Colpitts oscillator shown in Fig. 15 has been chosen. This common-collector configuration is well known, achieves low current consumption and allows placing a relatively big resonator (the microstrip and the adjustable capacitor in Fig. 15) physically apart from the other components of the oscillator. Although a current source is a good solution for biasing and quenching the oscillator, in this case the quench is applied through the base in order to reduce complexity and consumption. The quench is applied through an RF choke to avoid oscillator loading. The two capacitors C_1 and C_2 are equal in order to minimize the bias current necessary to cancel the circuit losses. The microstrip line acts as an inductance, whereas the capacitor CVAR (Murata TZC3, 2-6 pF) is adjustable for frequency tuning. The envelope detector, as the LNA, has been connected to the transistor base, where the oscillation exhibits greater amplitude. A connection to the emitter would reduce the loading effect of the envelope detector, at the price of a reduction in the detected amplitude.

Fig. 16 (a) shows the frequency response of the unloaded SRO (impedance at the base node) when the quench is disabled. The resonance takes place at 2.87 GHz, achieving a Q of 57 and maximum impedance of about 1000 Ω . A narrow

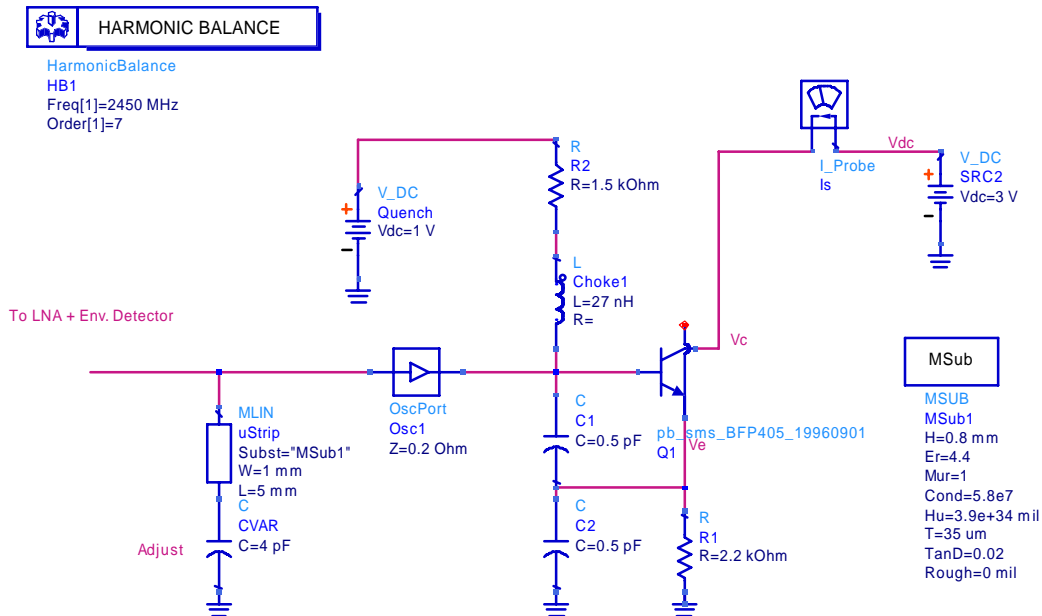


Figure 15. Schematic of the superregenerative oscillator.

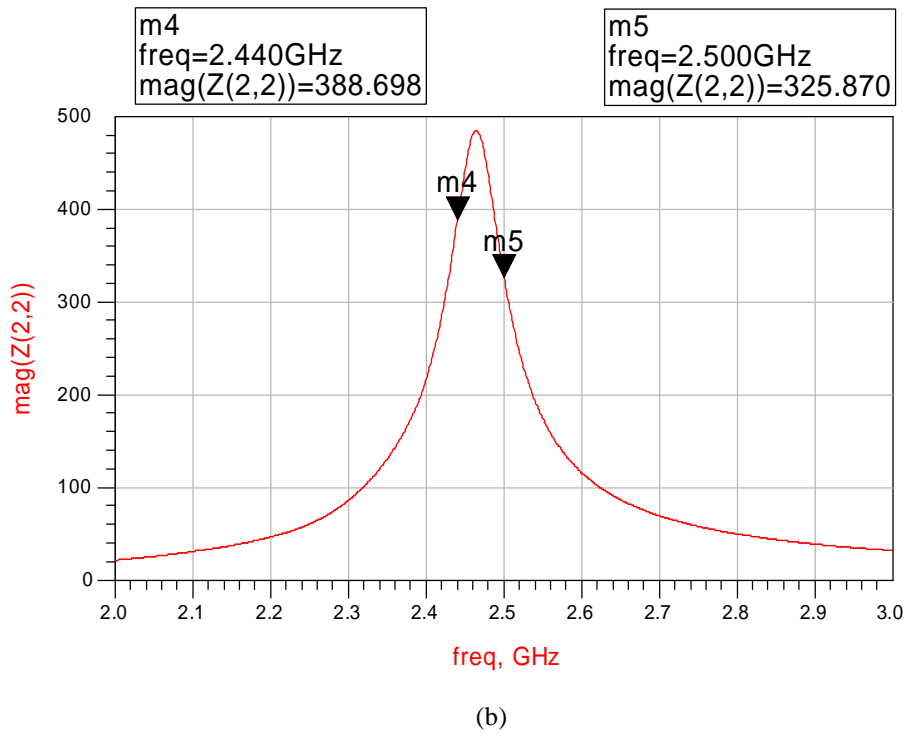
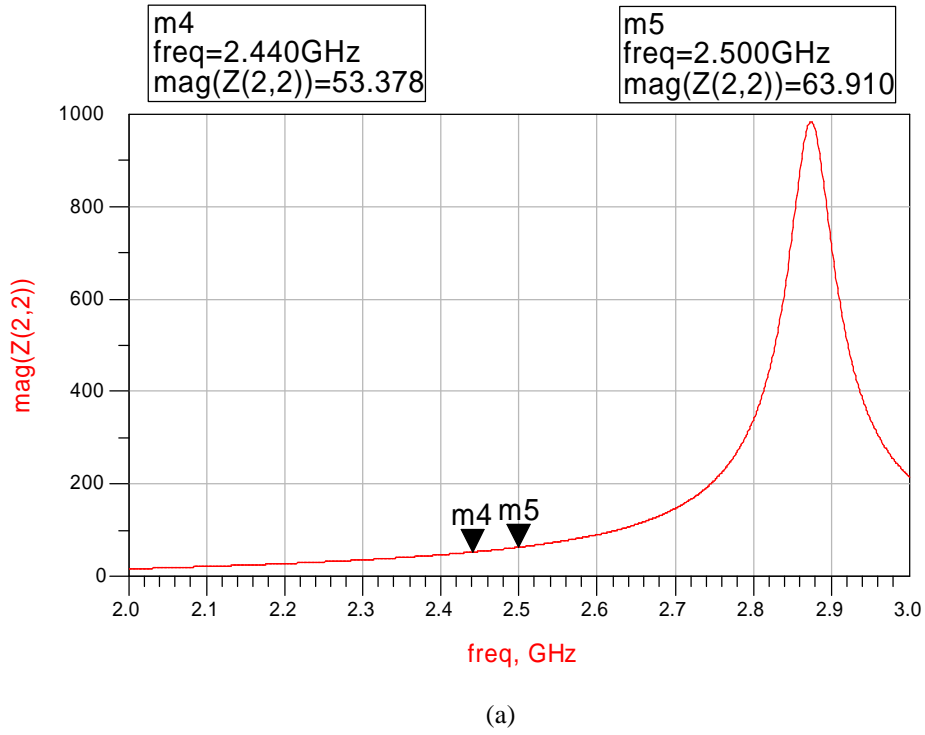


Figure 16. Module of the SRO impedance (ADS layout simulation): (a) unloaded; (b) loaded with the LNA and the envelope detector.

microstrip line (high characteristic impedance) increases the impedance at resonance, requiring a smaller collector current to compensate losses and produce oscillation (smaller critical current).

The frequency response of the loaded oscillator is shown in Fig. 16 (b). The resonant frequency f_0 decreases to 2.45 GHz, due to the output and input capacitances of the LNA and the envelope detector, respectively. The Q is reduced to 40, whereas the impedance at resonance is 500 Ω . Therefore, the critical current of the loaded oscillator increases with regard to the unloaded one. Fig. 17 shows the equivalent models for the different stages of the RF module. The model for the envelope detector belongs to the circuit presented in the next section.

Table 4 shows the influence of the microstrip dimensions on the impedance at resonance and the Q of the SRO. When the microstrip is enlarged, the resonance frequency increases, and so the length of the microstrip must be increased in order to obtain the same frequency. The size of the microstrip, which has been chosen for the SRO realization, is equal to 1 mm \times 5 mm. To get higher stability on the frequency of resonance, a ceramic coaxial resonator can be used instead of the microstrip line.

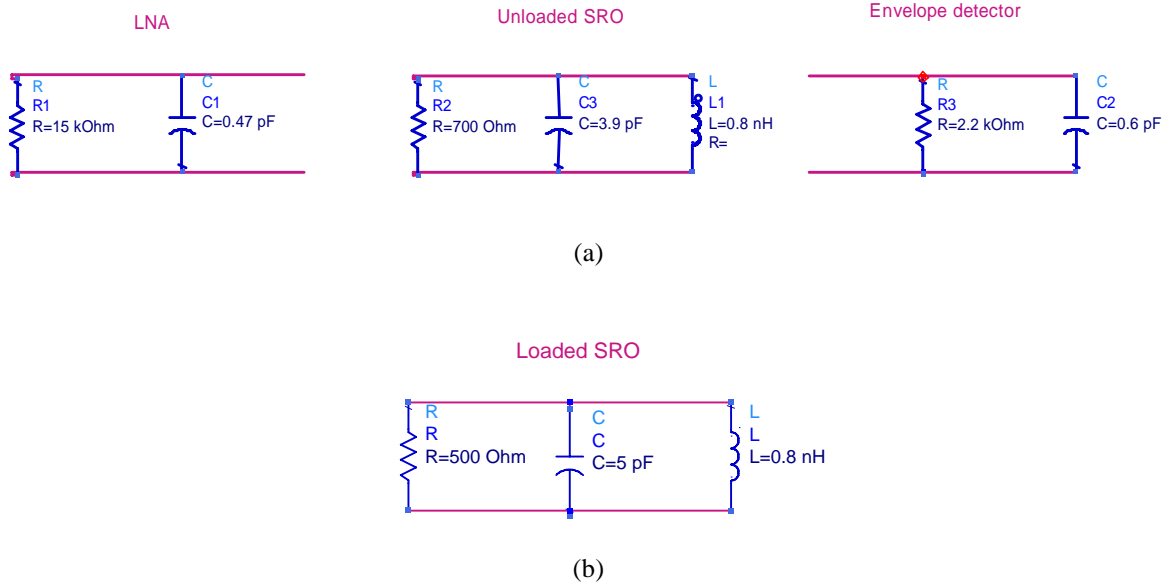


Figure 17. (a) Equivalent circuits for the LNA, the unloaded SRO and the envelope detector at the frequency of 2.45 GHz; (b) model for the loaded SRO.

Table 4. Sizes of the microstrip line providing a resonant frequency of 2.45 GHz (ADS layout simulation of the loaded SRO).

<i>Microstrip size</i> (mm ²)	$ Z _{\max}$ (Ω)	Q
1×5	485	38
2×7	455	38.5
3×8.5	420	39
4×9.5	380	40
6×11	300	41

2.6. Envelope detector

The envelope detector is the interface between the high-frequency and the low frequency part of the receiver. It is expected to accomplish the following requirements:

- To minimize the load to the SRO. In general, if the detection is achieved with a diode, a buffer will be necessary to separate the SRO from the diode load, which is nonlinear. Additionally, if the signal level in the SRO is small, amplification of the high frequency oscillation will be necessary to minimize the effect of the diode threshold.
- To provide an output level that can be easily amplified and processed.

Several configurations have been evaluated: a common-base amplifier plus a diode detector, a common-emitter amplifier plus a diode detector, and also the use of the transistor nonlinearity to generate an image of the envelope, as in [Fav-98]. In all these cases there is a common problem: obtaining an amplified version of the envelope requires large bias currents. For instance, Fig. 18 shows the signals that can be obtained with a common-emitter amplifier plus a conventional diode detector. The output pulse has a peak-to-peak amplitude of more than 0.5 V for an RF input amplitude of 100 mV. However, the current consumption is 7.5 mA.

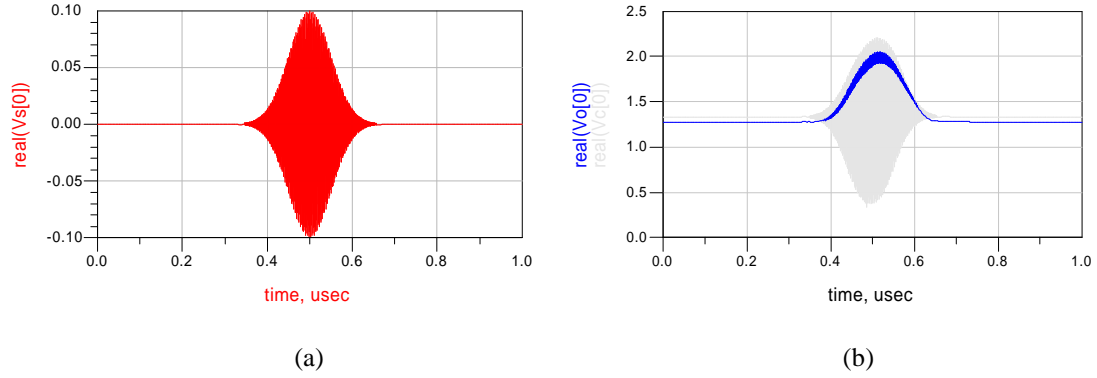


Figure 18. Signals in a common-emitter amplifier with BFP405 transistor ($I_c=7.5$ mA) plus a conventional envelope detector using low-threshold HSMS-2850 Schottky diodes: (a) RF input signal; (b) amplified RF signal and detected envelope.

Fig. 19 shows the schematic of the architecture that has been selected. It is a common-collector configuration where the transistor behaves as a diode that charges the capacitor CE2. The capacitor discharges through resistor RE2. Although this configuration does not amplify, it has the advantage of offering large input impedance, since the current necessary to charge the capacitor comes mainly from the collector, and not from the SRO. The network composed by CE3 and ChokeE1 serves to filter out the quench signal present at the input node (base of the transistor of the SRO). Eventually, an RF choke can be placed between the emitter of the transistor and the transmission line that connects it to the output connector of the PCB, to avoid the influence of the latter on the high-frequency side of the detector.

With bias currents below 50 μ A it is possible to achieve an input resistance of more than 10 k Ω and a detected envelope of 10-20 mV peak-to-peak. Nevertheless, Fig. 19 includes the values that maximize the output signal amplitude, providing 50 to 100 mV peak-to-peak. These values have been obtained experimentally and require a greater supply current of 140 μ A. Hence there is a compromise between output amplitude and current consumption. Fig. 20 shows the corresponding time signals for this latter case, whereas Fig. 21 plots the parallel input resistance and capacitance as a function of frequency.

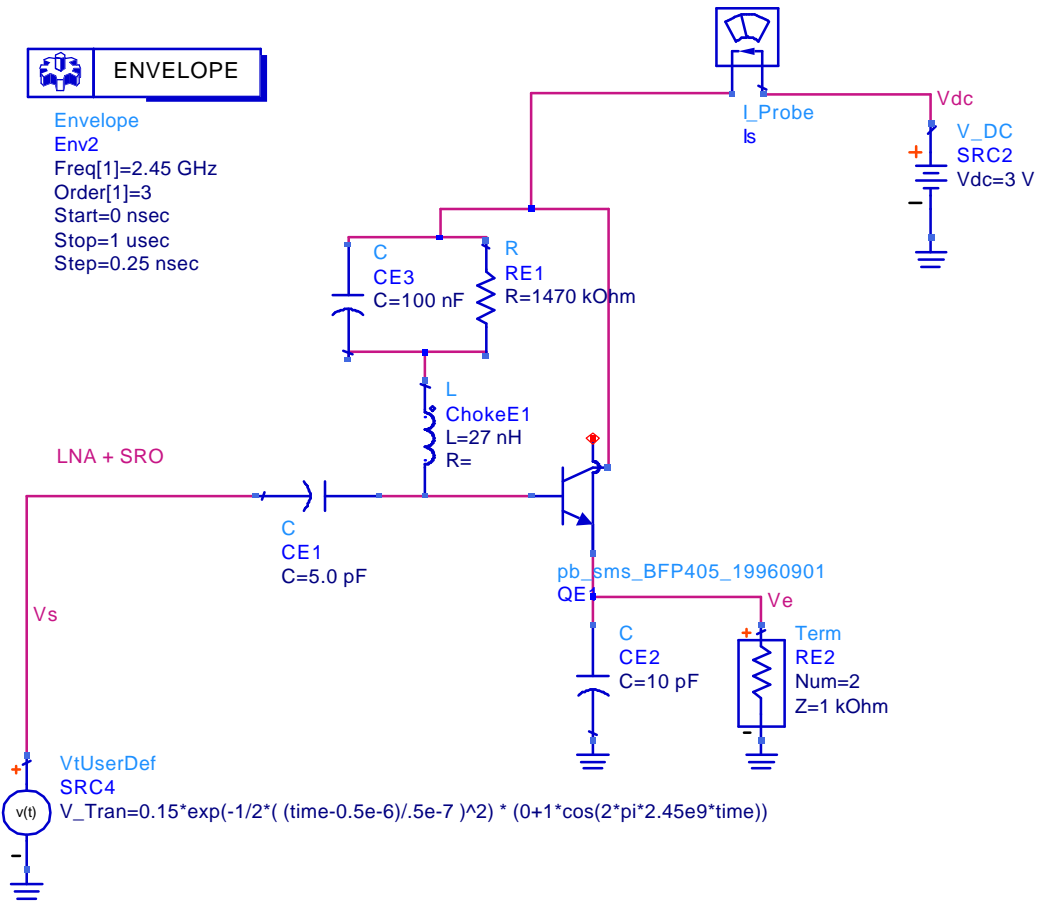


Figure 19. Schematic of the envelope detector.

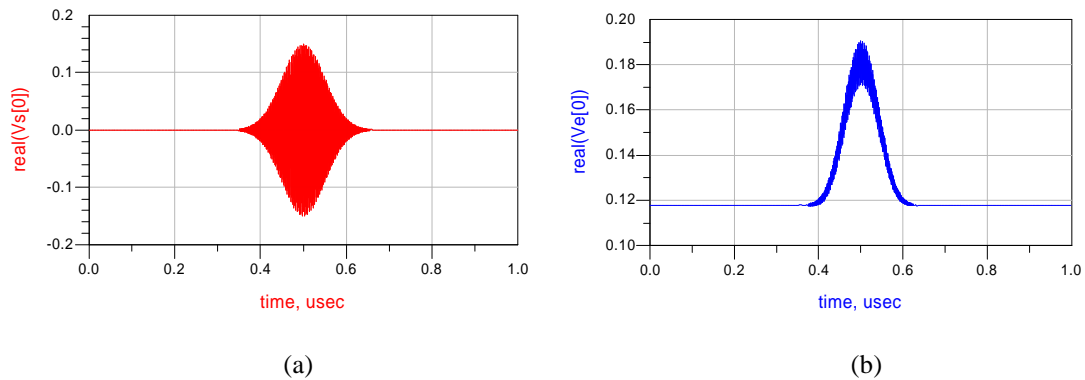


Figure 20. Signals in the implemented envelope detector using BFP405 transistor ($I_c=140 \mu\text{A}$): (a) RF input signal; (b) detected envelope.

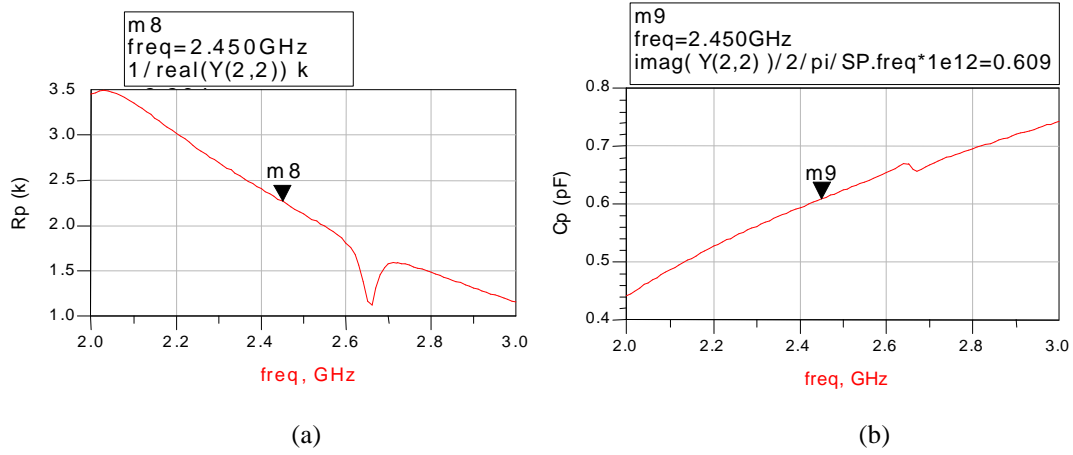


Figure 21. (a) Parallel input resistance of the envelope detector; (b) parallel input capacitance.

2.7. Implementation and experimental results

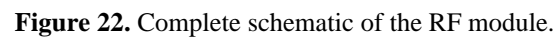
Fig. 22 shows the Protel Schematic of the RF module, and Fig. 23 shows the implemented PCB, on a 0.8-mm FR4 substrate.

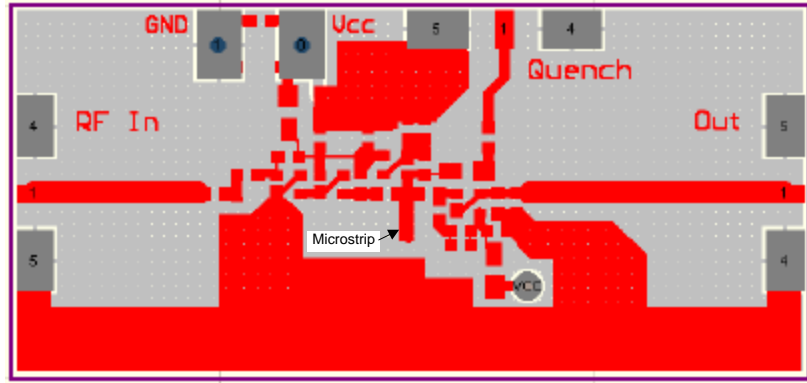
Fig. 24 shows the spectrum of the signal generated in the SRO without input signal (RF pulses grow up from noise, providing a continuous spectrum) and with input signal (discrete lines spaced by a distance equal to the quench frequency). A difference of about 30 MHz is observed between the reception center frequency and the frequency of the generated oscillation. This is likely due to the change of the parasitic capacitances of the SRO transistor as the quench voltage increases.

Fig. 25 shows the applied quench voltage and the detected envelope for sinusoidal and sawtooth quench.

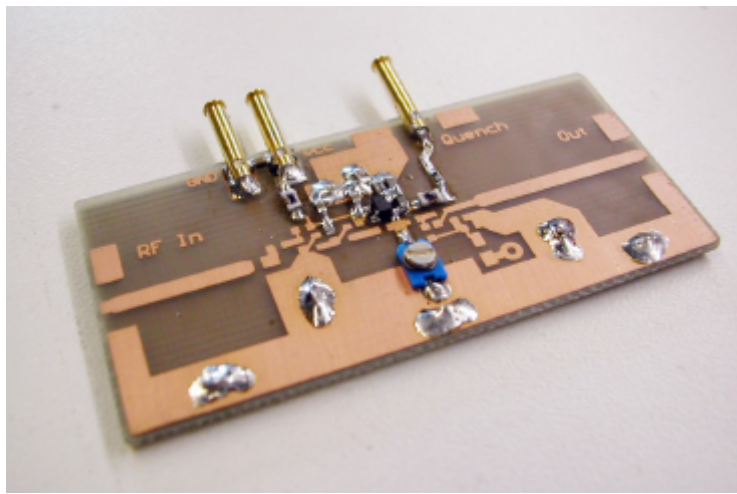
Fig. 26 shows the frequency response of the receiver for 1-MHz and 10-MHz quench frequency. The applied quench is sinusoidal, considering two extreme situations: small quench amplitude, with the mean bias current near to the critical value, and with large quench amplitude. It has also been confirmed that the sawtooth quench provides a more selective response, especially when small quench amplitude is applied. Concretely, the -3 dB bandwidth in this case for 1-MHz quench frequency is 4 MHz instead of 5 MHz.

A phenomenon of hysteresis with regard to both the input amplitude and the mean quench current is observed when the receiver is slightly superregenerative (mean

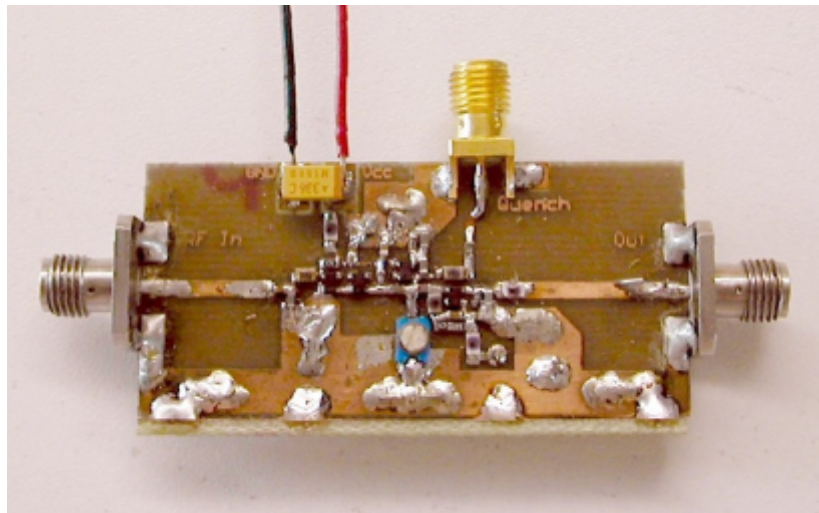




(a)

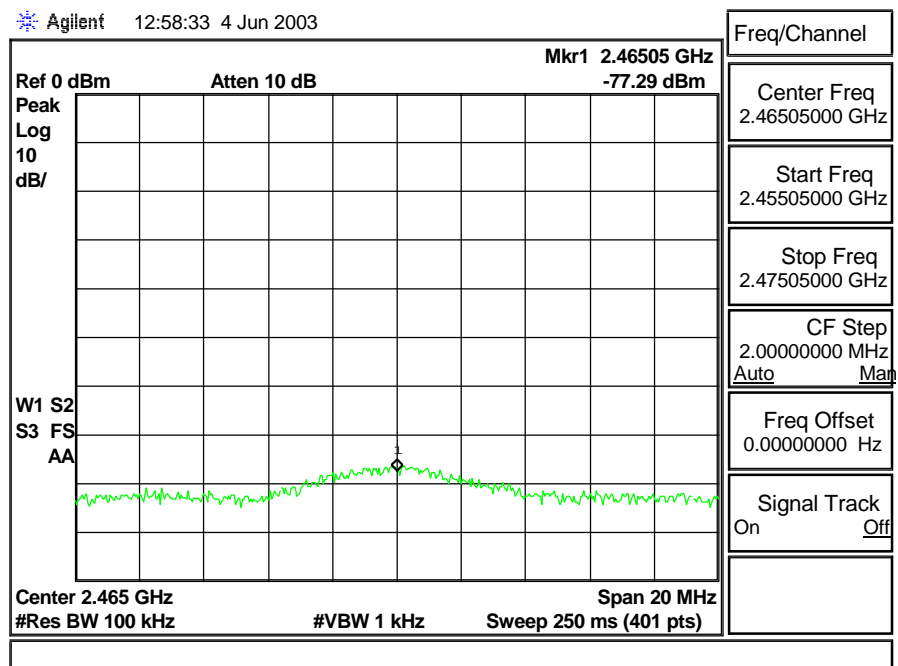


(b)

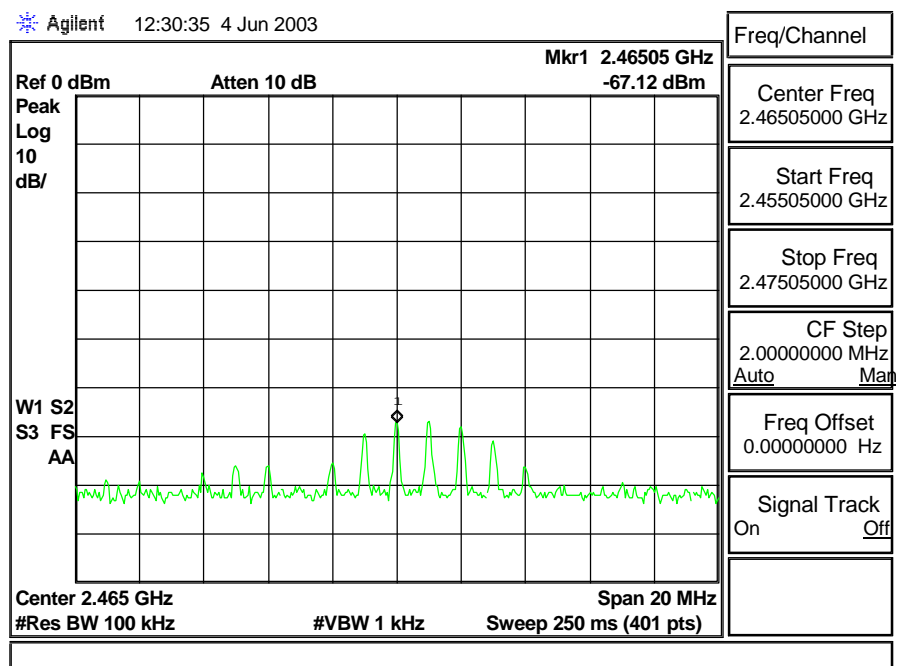


(c)

Figure 23. (a) Layout of the RF module; (b) an implementation for the evaluation of the unloaded SRO; (c) complete module with the LNA, the SRO and the envelope detector.

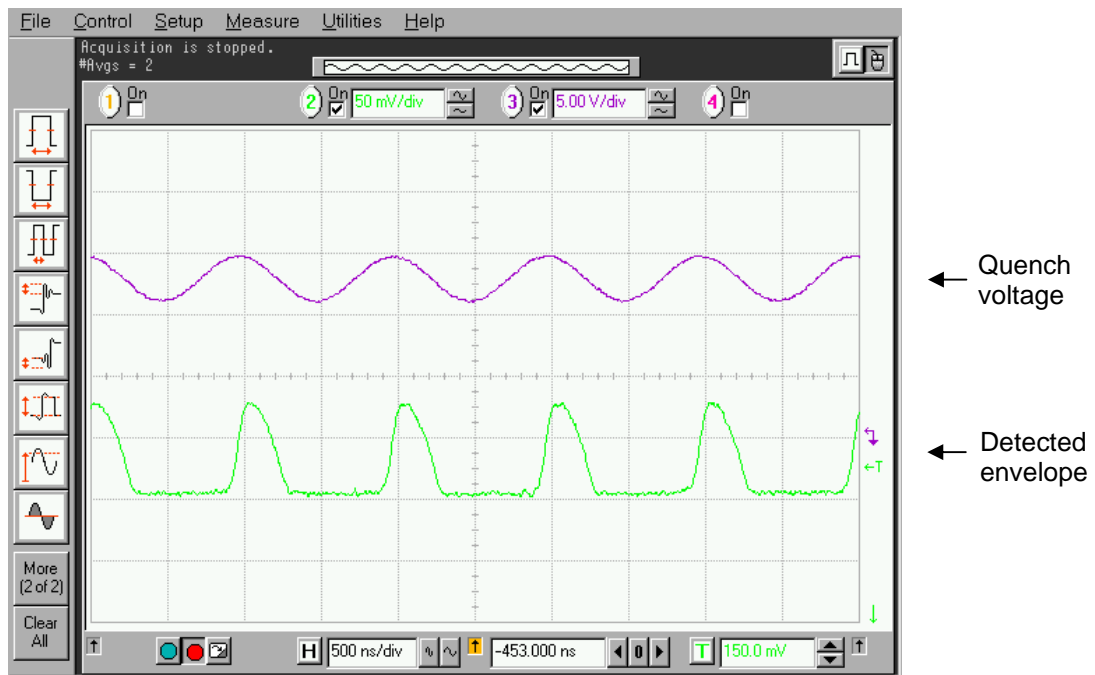


(a)



(b)

Figure 24. Spectrum of the signal generated in the SRO: (a) in the absence of signal; (b) in the presence of a -85 dBm tone tuned to the reception center frequency.

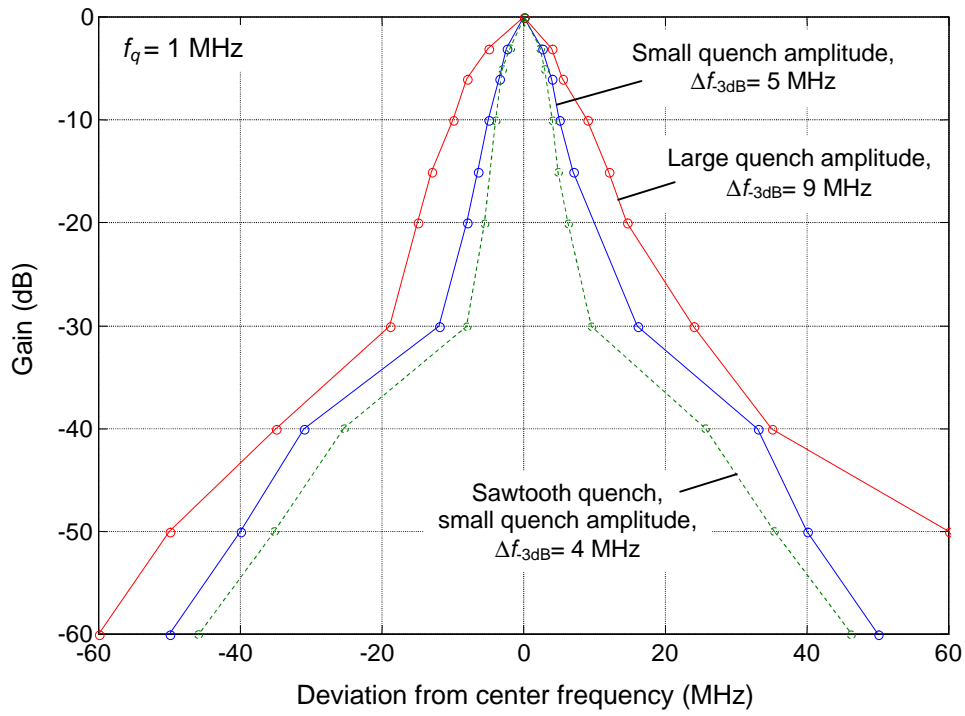


(a)

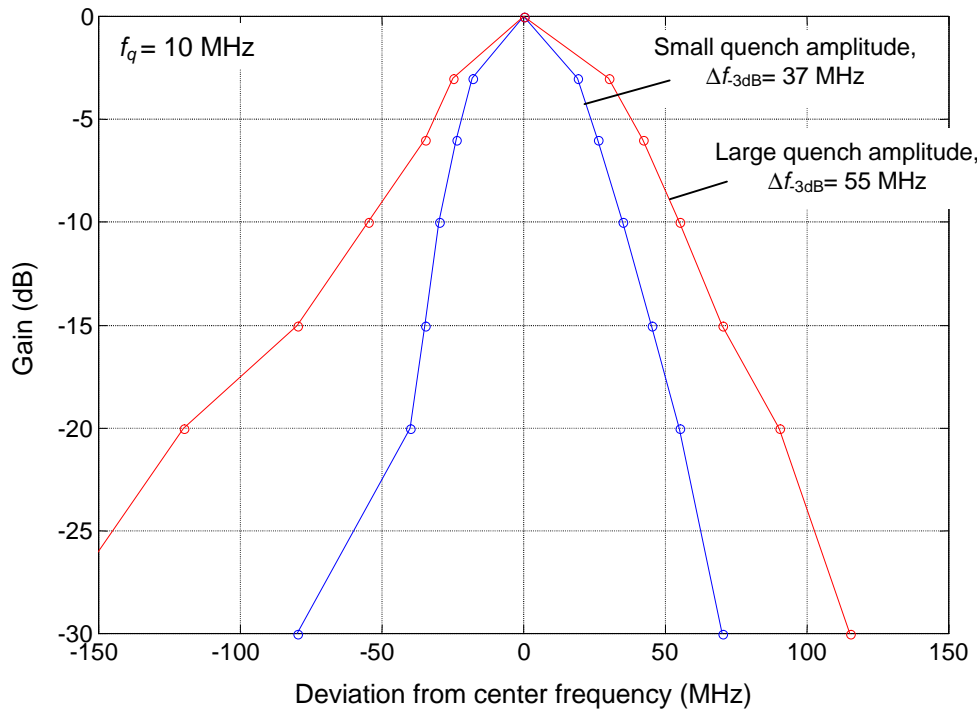


(b)

Figure 25. Quench voltage and detected envelope in the presence of a -85 dBm tone tuned to the reception center frequency: (a) sinusoidal quench; (b) sawtooth quench.



(a)



(b)

Figure 26. Measured frequency response of the receiver with sinusoidal quench (unless otherwise noted) and a quench frequency of (a) 1 MHz and (b) 10 MHz.

quench current too near to the critical current). For instance, the pulses generated in the SRO disappear when the RF input level decreases below -95 dBm coming from a high level, and they appear when the level increases to -92 dBm coming from a low level. Hence, to avoid this phenomenon, care must be taken to assure a certain gap between the mean quench current and the critical current. The hysteresis tends to disappear as the quench frequency is increased. It has not been observed in the unloaded SRO.

A version of the unloaded SRO using BFP420 transistor has been evaluated. This transistor, as the BFP405, exhibits an outstanding high-frequency response and was available in the evaluation kit of Infineon Technologies. However, it has greater parasitic capacitances (see Table 1) and requires greater bias current to achieve the same gain. These characteristics have been verified experimentally: the oscillation frequency decreases 300 MHz with BFP420 and the critical current increases about $30 \mu\text{A}$. So, the BPF405 shows up as a better choice.

Fig. 27 shows the peak-to-peak output voltage provided by the envelope detector as a function of the RF input level.

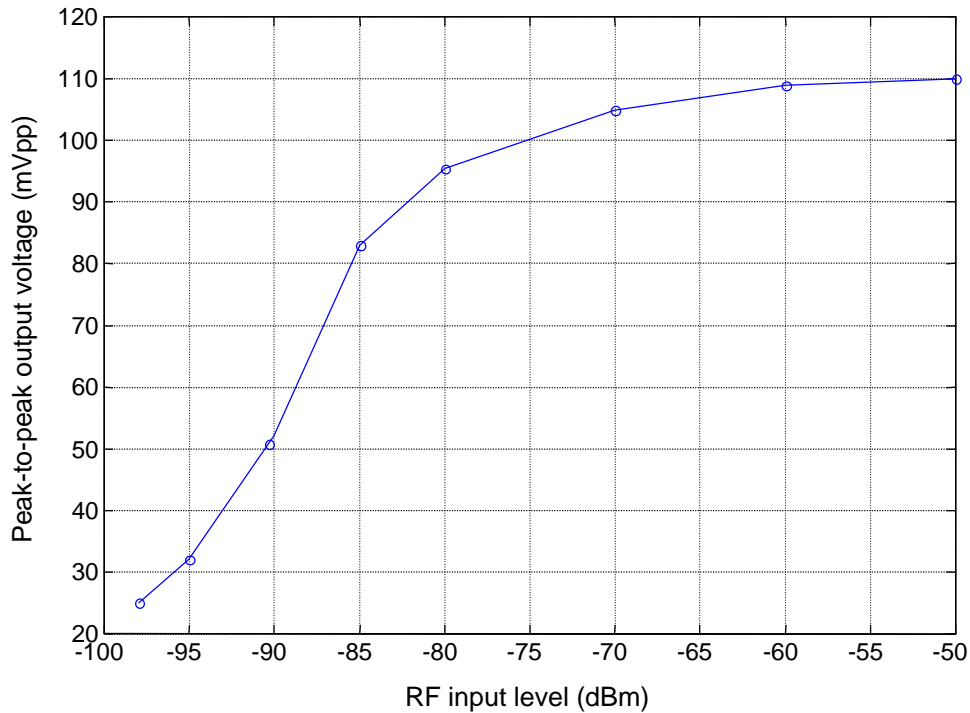


Figure 27. Peak-to-peak amplitude of the detected envelope versus RF input level ($f_q=1$ MHz, sinusoidal quench). The receiver gain has been adjusted to provide 50 mVpp with an RF input level of -90 dBm.

Table 5 shows the main characteristics of the LNA, the SRO and the envelope detector, whereas Table 6 summarizes the overall performance of the RF module. The received modulation is OOK with constant bit envelope. The receiver is quenched one time per bit period using sinusoidal quench.

Table 5 – Characteristics of the RF stages at 2.45 GHz.

<i>Parameter</i>	<i>Value</i>	<i>Unit</i>
LNA		
Noise figure	2.5 ⁽¹⁾	dB
Gain	27 ⁽¹⁾	dB
Reverse isolation	40 ⁽¹⁾	dB
Supply current	460	μA
SUPERREGENERATIVE OSCILLATOR		
Operating frequency	2.2 - 2.8	GHz
Loaded Q	28	
Maximum quench frequency	18	MHz
Supply current		
at $f_q=1$ MHz	70 - 150 ⁽²⁾	μA
at $f_q=10$ MHz	270 - 470 ⁽²⁾	μA
ENVELOPE DETECTOR		
Peak-to-peak output voltage	30 - 110	mV
Supply current	140	μA

Table 6 – Overall performance at 2.45 GHz.

<i>Parameter</i>	1-Mbps data rate	10-Mbps data rate	<i>Unit</i>
-3 dB bandwidth	5 - 9 ⁽²⁾	37	MHz
Sensitivity level (BER= 10^{-3})	-95 to -90 ^{(2) (3)}	-82 to -80 ⁽²⁾	dBm
Total supply current	670 - 750 ⁽²⁾	870 - 1070 ⁽²⁾	μA

⁽¹⁾ Values obtained with ADS layout simulation.

⁽²⁾ Depending on mean quench current.

⁽³⁾ Down to -98 dBm in regenerative mode.

3. LOW-FREQUENCY PART AND COMPLETION OF THE RECEIVER

Due to time restrictions, the Single-Flank Delay-Locked Loop has been chosen to achieve the synchronous operation of the receiver, thanks to its noteworthy simplicity. Fig. 28 shows the complete block diagram of the receiver, where the low-frequency part includes a low-frequency amplifier, the loop filter and the quench VCO.

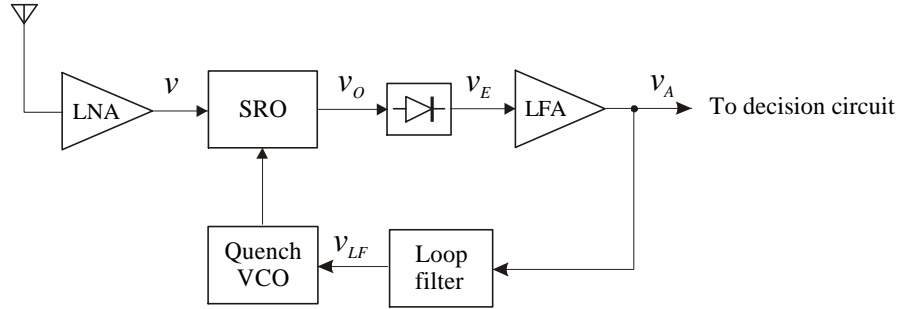


Figure 28. Block diagram of the implemented receiver, based on the Single-Flank Delay-Locked Loop technique.

3.1. Low-frequency amplifier, loop filter and quench VCO

Fig. 29 (a) shows the schematic of a dual-stage non-inverting low-frequency amplifier using high-beta BC109C transistor. This configuration has served to proof the new concept presented in this work, i.e., the synchronous operation of the superregenerative receiver, concretely at 1 Mbps. However, the speed of this transistor is not very good, requiring a large biasing current (400 μ A for the first stage plus 3.4 mA for the second one).

A much better result is obtained with BFR93A RF transistor, which provides faster response with lower biasing currents. Fig. 29 (b) shows a single-stage inverting amplifier that has been evaluated. The signal inversion implies that the synchronization loop will operate on the descending flank of the received bit, instead of the ascending one. This amplifier is suitable until 10 Mbps and above. Because of the single-stage configuration, the current consumption is reduced. Table 7 shows the parameters required to provide a 2-V_{pp} output voltage from a 50-mV_{pp} input amplitude. A capacitive load of 10 pF is considered, representing the input capacitance of the

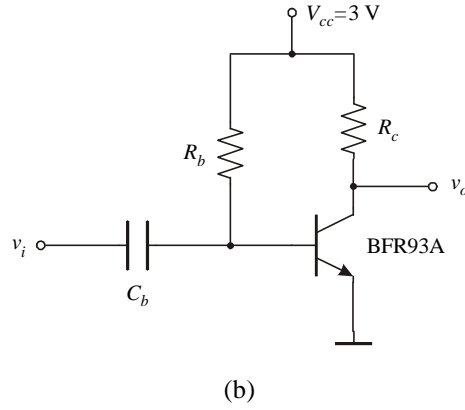
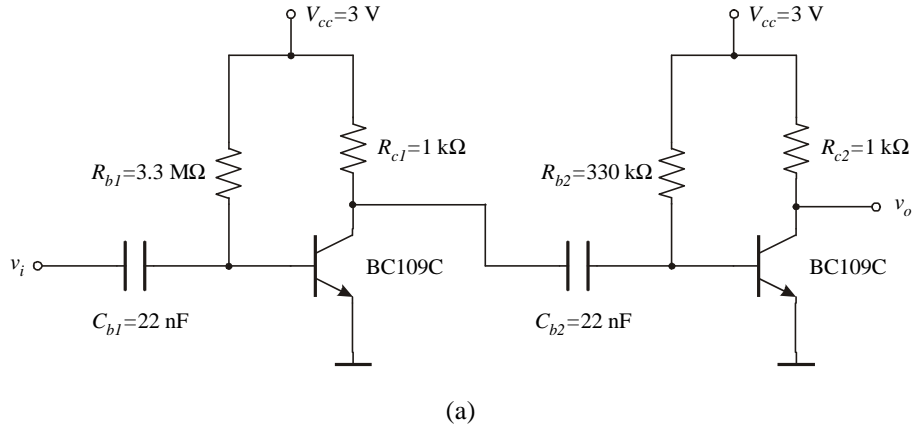


Figure 29. (a) Non-inverting low-frequency amplifier for 1-Mbps data rate using high-beta BC109C transistor; (b) inverting amplifier for high data rates with BFR93A.

Table 7. Parameters providing a 2-V_{pp} output voltage from a 50-mV_{pp} input voltage in the circuit of Fig. 29 (b), with a grounded capacitive load of 10 pF.

Data rate (Mbps)	C (nF)	R_b (k Ω)	R_c (k Ω)	Supply current ⁽¹⁾ (mA)
1	22	1800	8.2	0.12
10	2.2	180	1.0	1.00

⁽¹⁾ Average current with equiprobable one and zero bits.

decision stage. The current consumption of this amplifier is approximately proportional to the value of the load capacity. Hence, depending on the particular load and the peak-to-peak amplitude required for the bit detection, the consumption of the amplifier can be reduced significantly. Fig. 30 shows the SPICE simulation of the amplifier response at 10 Mbps.

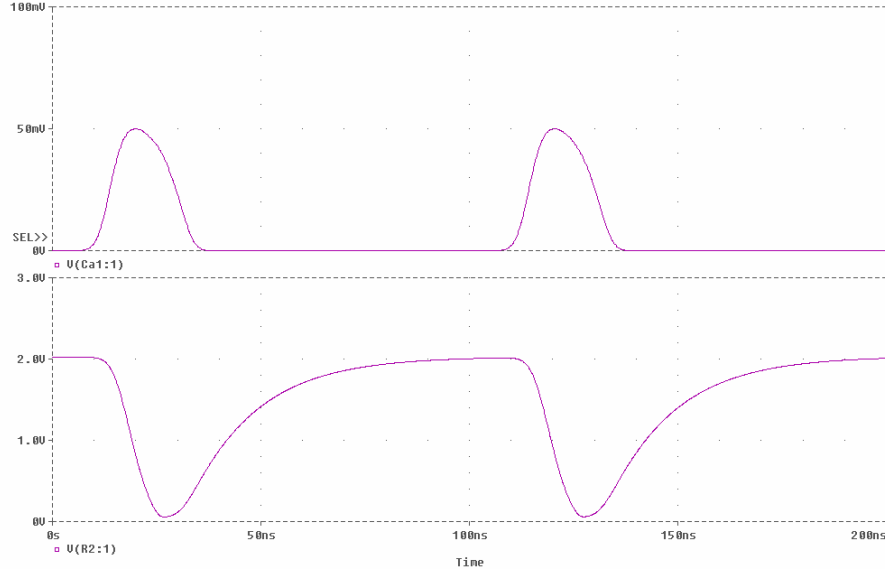


Figure 30. SPICE simulation of the input and output signals of the amplifier in Fig. 29 (b), at 10 Mbps and with a capacitive load of 10 pF.

The use of BFP405 has also been considered for the low-frequency amplifier, due to its outstanding response at low biasing currents; however, experiments have demonstrated a clear trend to generate undesired oscillations.

Fig. 31 shows the complete schematic of the low-frequency part of the final implementation of the receiver. Next to the LF amplifier, a DC restorer (clammer) composed by CCLAMP and DCLAMP has been included to fix the upper base line of the output signal. This clamper helps to generate a DC component at the output of the loop filter that is more sensitive to the input-signal level. The loop filter is a first-order lowpass RC filter, with a bandwidth of approximately $f_b/10$ (f_b =bit rate). Its relatively large time constant ensures the integration of many bit pulses, in order to allow bursts of a certain number of contiguous ones or zeros without introducing appreciable fluctuations in the frequency of the VCO. The use of this filter, however, is not mandatory, since the VCO itself performs a lowpass filtering of the control signal. The adjustable resistor RLF3 serves to modify the amplitude of the VCO control signal, and, therefore, the loop gain. Finally, the quench VCO is a grounded-base version of the Colpitts oscillator, where CVCO2, CVCO3 and LVCO must be chosen properly to operate at the desired frequency. The SRO is AC coupled to the emitter of the transistor because of its low output impedance. The potentiometer RQ2 serves to fix the bias current of the SRO.

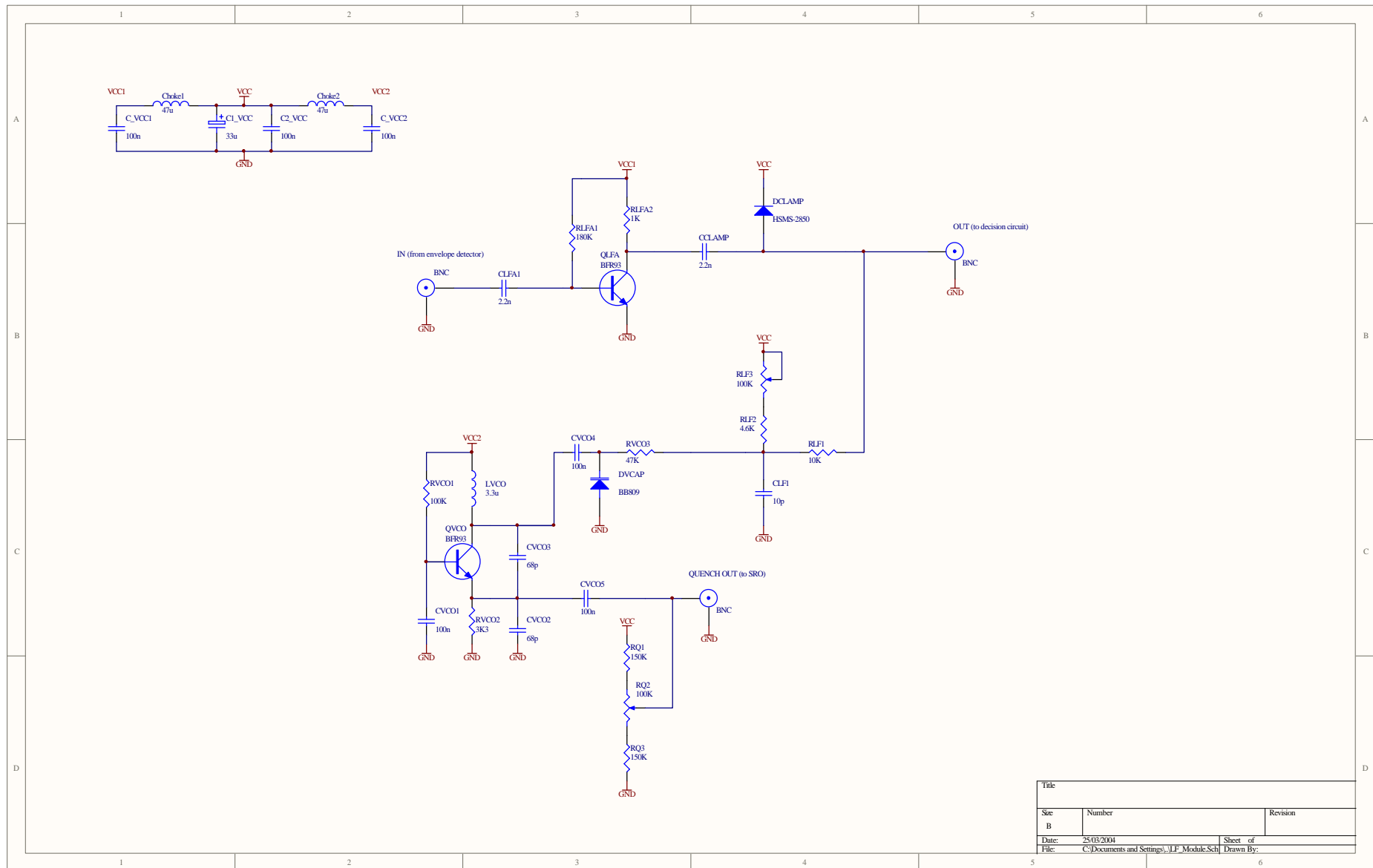


Figure 31. Complete schematic of the LF module for operation at 10 Mbps; the following values must be changed to operate at 1 Mbps:

RLFA1=1.8 M Ω , RLFA2=8.2 k Ω , CLF1=150 pF, RVCO2=6.8 k Ω , CVCO2=CVCO3=820 pF and LVCO=47 μ H.

3.2. Measurements and experimental results

Fig. 32 shows the signals generated in the closed-loop receiver at 1 Mbps (these oscillograms have been obtained with an external VCO generating sawtooth quench). In this case, the LF amplifier in Fig. 29 (a) has been used. This amplifier does not require a clamper. A 74HC123 monostable multivibrator has been used as a decision circuit. In Fig. 32 (a) the received data are a periodic alternation of ones and zeros. It has been verified that a return-to-zero bit envelope, such as the Gaussian shape, improves the synchronization capability of the receiver. In this case, the Gaussian envelope matches (approximately) the sensitivity curve of the SRO, at the price of an increased bandwidth in the transmitted signal. Fig. 32 (b) shows how the receiver supports alternated bursts of ones and zeros, provided that a certain balance between zeros and ones exists.

Fig. 33 shows the signals obtained with the final circuit in Fig. 31 at 10 Mbps. At this bit rate, the amplitude generated by the quench VCO, of about 1.2 V, is not high enough to drive the SRO in Fig. 22. To solve this problem, resistor R2 in Fig. 22 has been decreased from 1.5 k Ω to 330 Ω . A 74HC14 Schmitt trigger has served in this case to retrieve the data. This circuit increases the total supply current by 250 μ A.

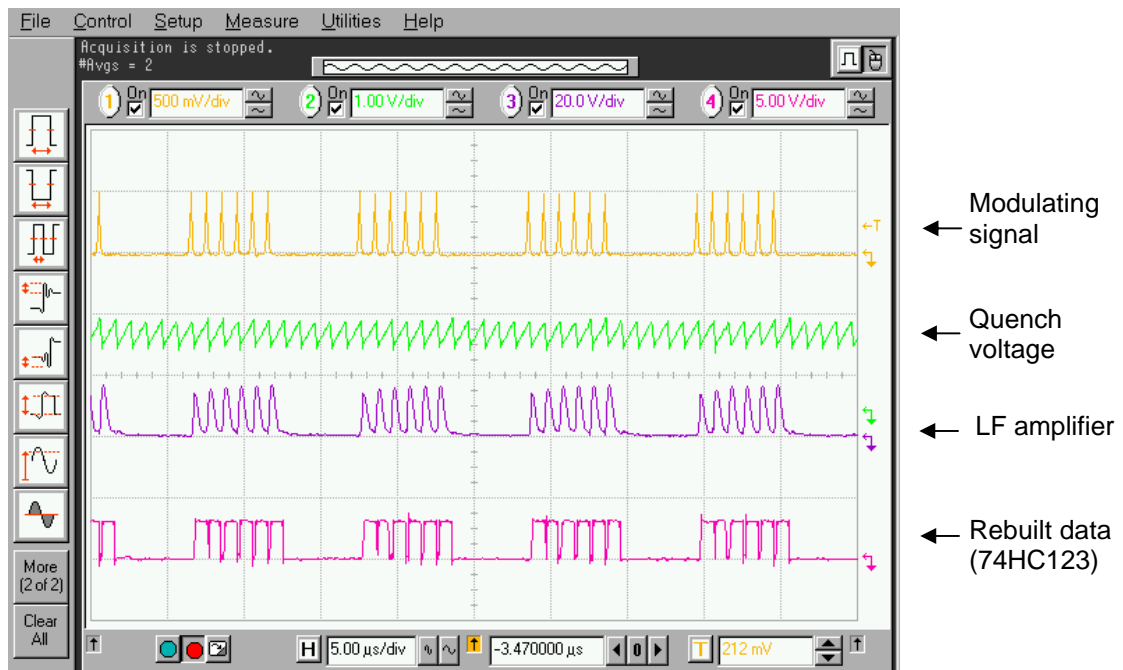
Table 9 summarizes the performances of the closed-loop receiver (final design) at 1 Mbps and 10 Mbps. The acquisition and tracking ranges of the VCO are about 0.2-0.3 % of its oscillation frequency. As expected, the tracking range is always greater than the acquisition range. It has been verified that the acquisition and tracking ranges increase with loop gain. However, an excessive gain causes a noteworthy jitter to appear. Beyond a certain value, the loop becomes unstable and unable to synchronize. As shown in Table 8, the synchronization loop can operate at RF input levels quite lower than those required to have an acceptable bit error rate.

The input-signal dynamic range is quite larger at 1 Mbps. However, the corresponding values are not as good as those obtained in spread-spectrum applications [Mon-02]. When a VCO frequency correction is applied, the dynamic range increases. VCO frequency correction means that the free oscillation of the VCO is modified for each input-signal level in order to obtain an optimum operating point.

Finally, Table 10 shows the distribution of the current consumption in the receiver. A total consumption below 1 mA at 1 Mbps and 2.5 mA at 10 Mbps is feasible.



(a)



(b)

Figure 32. Signals at 1 Mbps: (a) data signal composed by alternated ones and zeros; (b) data signal composed by alternated bursts of ones and zeros.

Table 8. Features of the complete receiver.

<i>Parameter</i>		1-Mbps data rate	10-Mbps data rate	<i>Unit</i>
Modulation		OOK, Gaussian bit envelope		
Quench type		Sinusoidal		
Reception center frequency		2450		MHz
Loop-filter bandwidth		100	1600	kHz
VCO frequency-deviation constant		30	200	kHz/V
Sensitivity level (BER= 10^{-3})		-93	-81	dBm
Minimum synchronization level		-106	-100	dBm
Bit-frequency acquisition / tracking range				
dB above sensitivity level	+10 dB	0.9 / 1.9	16 / 42	kHz
	+20 dB	1.3 / 2.7	30 / 86	kHz
Input-signal dynamic range				
without VCO freq. correction		45	10 - 15	dB
with VCO freq. correction		65	30	dB
Total power consumption		3.0	6.9	mW

Table 9. Distribution of the consumption in the receiver in μ A.

<i>Block</i>	1-Mbps data rate	10-Mbps data rate
LNA	460	460
SRO	100	270
Envelope detector	140	140
Quench VCO	170	430
LF amplifier	120	1000
TOTAL	990	2300

4. CONCLUSIONS

In the present work, a synchronous superregenerative receiver operating in the 2.4-GHz ISM band has been evaluated. The prototype has demonstrated that the synchronous operation of the receiver yields a significant number of advantages, namely:

- 1) *Increased data rate*, since the synchronous operation implies that the data rate equals the quench frequency, and no longer a fraction of it. In particular, 10 Mbps (potentially up to 18 Mbps with proper design of the low-frequency part) represents a record in this type of receiver.
- 2) *Improved selectivity*. The RF bandwidth of the receiver is much closer to the bandwidth of the received signal, overcoming one of the traditional drawbacks of the receiver. An example of this improvement is the RF bandwidth of 37 MHz for a 10-Mbps data rate, a ratio of 3.7, whereas for conventional receivers the ratio is typically greater than 10 [Vou-01] [Joe-01].
- 3) *Improved sensitivity*. The use of special bit envelopes allows the bit energy to be concentrated in the sensitivity periods of the receiver. In this way, the receiver can make more efficient use of the incoming signal power, at the price of an increased bandwidth in the transmitted signal.
- 4) *Simplicity*. Indeed, the proposed architecture gives rise to implementations that are even simpler than conventional receivers. The main reason is that the synchronous receiver does not require the high-order lowpass filter that is commonly used in conventional receivers to remove the quench components.
- 5) *Supplied data clock*. In the asynchronous mode of operation, a clock recovery circuit is necessary to retrieve the bit synchronism from the data signal itself. On the contrary, when the receiver is quenched synchronously with the received data, the quench signal serves as a reference clock for the bit detection.

There are also two major problems that have been observed during the evaluation of the receiver:

- 1) *Operation under constant signal-to-noise ratio*. With the Single-Flank DLL technique, the average signal level at the envelope detector output (and so the

control signal of the quench VCO) is independent of the input signal level. The reason is that the loop advances or delays the phase of the quench VCO to regulate the amount of input signal power that falls into the sensitivity period. This ensures that, in the steady state of operation, the control signal of the VCO exhibits a fixed level, necessary to maintain the loop in lock. This property can be seen as an advantage, since the receiver output becomes independent of the input signal level within a range of typically 30 to 50 dB. However, it is also an inconvenience: an increase in the input signal level will not result in an improvement of the quality of reception. For instance, if the loop is adjusted to deliver optimum performance with an RF input level of -90 dBm, the signal-to-noise ratio at the SRO output will remain the same with -60 dBm. The solution to this problem remains as a future research line. On the other hand, the synchronization via architectures that take into account the two flanks of the received bit, such as the TDL, must be evaluated. According to results obtained with spread-spectrum receivers, the TDL shows up less sensitive to the input signal level than the Single-Flank DLL [Mon-02].

- 2) *Data jitter*. Although theoretically the data jitter should be small due to the synchronous operation of the receiver, it has been appreciable in practice, especially when the loop gain is high (for instance, with high VCO deviation constant). The jitter can be reduced by lowering the VCO deviation constant, at the price of a reduction of the frequency capture range.

It must be mentioned, as a final remark, that the design of the high-frequency part of the receiver has been the most costly and time consuming.

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My gratitude to Norbert Joël for advice in the design and implementation of the different blocks of the receiver, and to Jari-Pascal Curty and Frédéric Castella for critical help in the design of the high-frequency part of the receiver.

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